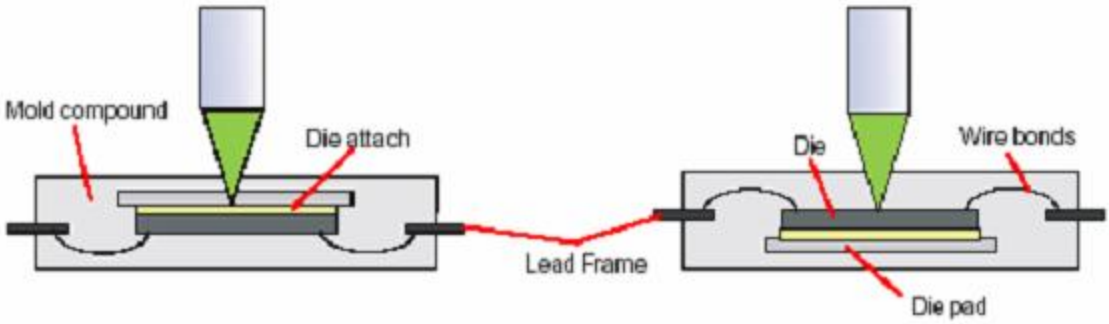
IC inspection

PlasticIC packaging accounts for almost 80% of the worldwide packaging market. Improvements in materials, in terms of encapsulants with low-ionic content and low stress, have significantly enhanced the environmental and mechanical reliability of plastic packages.

Die attach is required in all IC packages to attach the silicon chip to the package. Die attach may also provide an electrical connection to the silicon bulk, and in VLSI applications, it provides the main heat flow path from the silicon die to an external heat sink or ambient. The die-attach layer must also minimize the temperature coefficient of expansion mismatch between the silicon and the package. As the area and power dissipation of silicon chips continues to increase, the integrity of this layer becomes increasingly critical.

Tape automated bonding (TAB) in an IC-packaging technology that offers advantages in high-circuit density, a low profile, and a facility to test devices immediately prior to assembly. Although flip-chip attachment is now regarded as a viable alternative, because of its attributes, TAB is finding increasing application in low-profile consumer products, smart cards, liquid crystal displays, and in assembling high pin count ICs for use in high-performance computer products.

The microelectronics industry has a continuing need for rapid turnaround, user friendly, nondestructive analysis capabilities to assess the integrity and performance of packaging and interconnection technologies.
The developments in the field of scanning acoustic microscopy offer today a great possibility to analyze different kinds of microelectronic-packaging technologies.



Schema of an IC, the scanning acoustic microscopy is able to make the different parts of an IC visible.

IC inspection

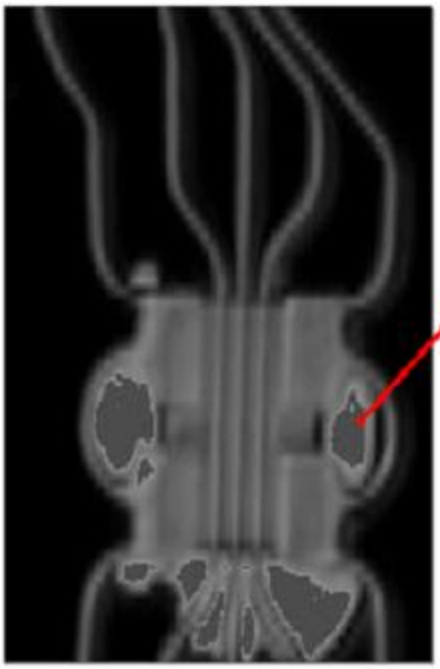


Fig. a

Automated failure detection due to phase inversion algorithm.
Delaminations are visible in red color.

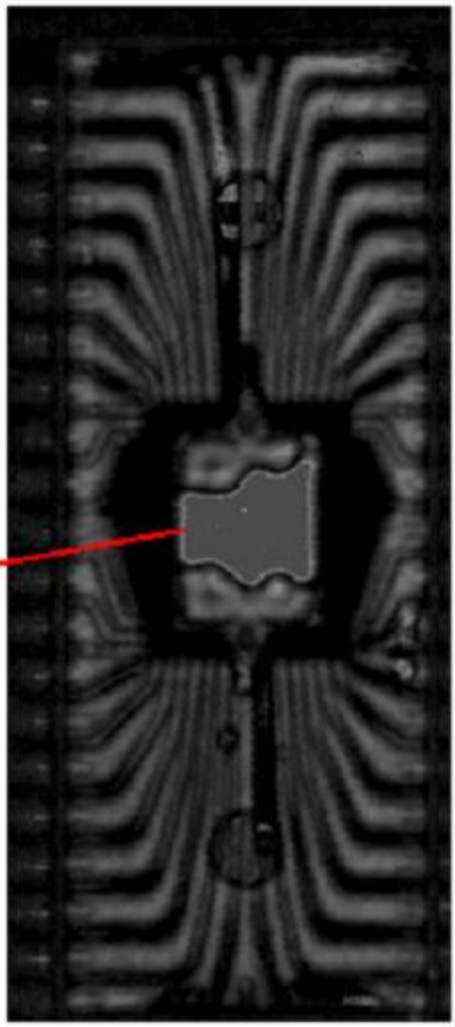


Fig. b